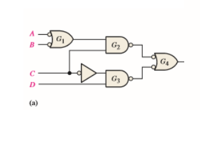
**Write down the Boolean expression of the following circuit .Give the output wave form of each gate in the diagram.**



* **BOOLEAN EXPRESSION:**

[(A’+B’) . C] + [C’ . D]

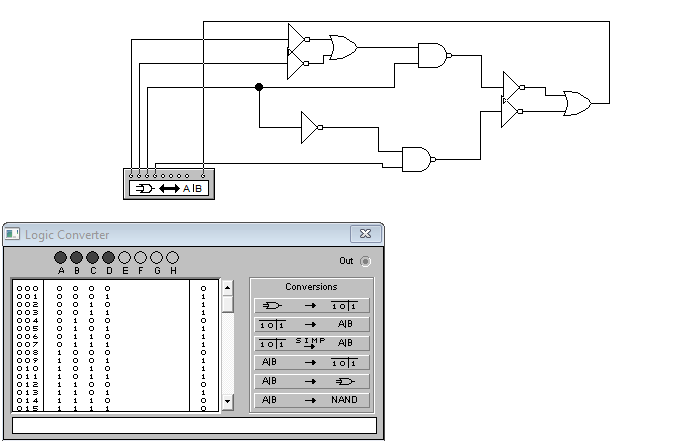
* **TRUTH TABLE :**

**LET ,**

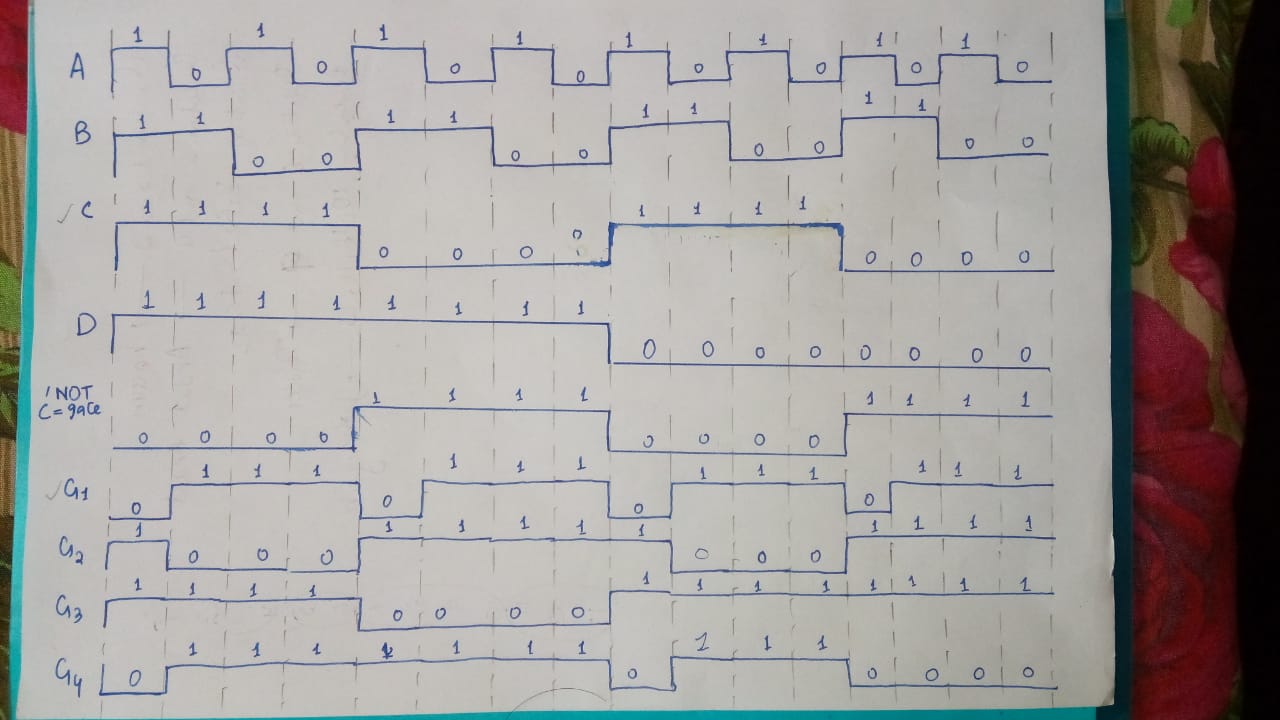
F=[(A’+B’) . C] + [C’ . D] , P=[(A’+B’) . C] , Q=[C’ . D]

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **A’** | **B’** | **C’** | **A’ + B’** | **P** | **Q** | **F** |
| **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **1** |
| **0** | **1** | **0** | **0** | **1** | **0** | **1** | **1** | **0** | **0** | **0** |
| **0** | **1** | **0** | **1** | **1** | **0** | **1** | **1** | **0** | **1** | **1** |
| **0** | **0** | **1** | **0** | **1** | **1** | **0** | **1** | **1** | **0** | **1** |
| **0** | **0** | **1** | **1** | **1** | **1** | **0** | **1** | **1** | **0** | **1** |
| **0** | **1** | **1** | **0** | **1** | **0** | **0** | **1** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **0** | **0** | **0** |
| **1** | **0** | **0** | **1** | **0** | **1** | **1** | **1** | **0** | **1** | **1** |
| **1** | **1** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** |
| **1** | **1** | **0** | **1** | **0** | **0** | **1** | **0** | **0** | **1** | **1** |
| **1** | **0** | **1** | **0** | **0** | **1** | **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **1** | **1** | **0** | **1** | **0** | **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

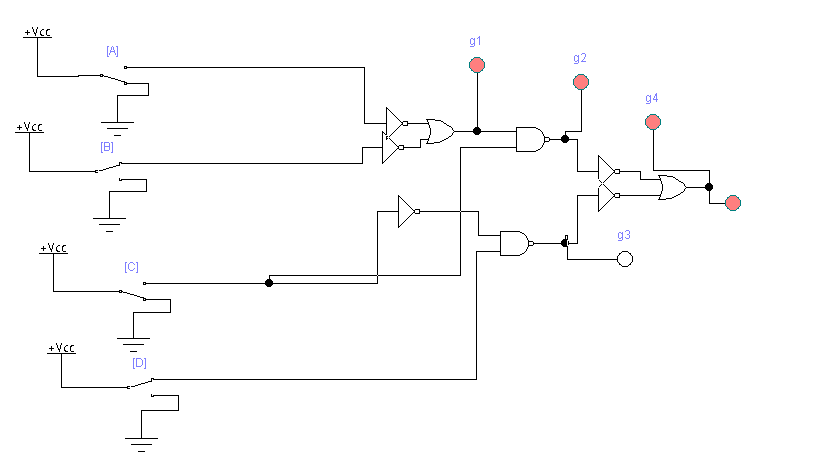
* **VERIFIACTION THROUGH LOGIC CONVERTER:**



* **OUTPUT WAVEFORM FOR EACH MENTIONED GATE :**

****

* **VERIFIACTION OF WAVEFORM THROUGH CIRCUIT SIMULATION:**



**QUESTION NO : 5 (b)**

**Explore a logic circuit with four input variables that will only produce a 1 output when**

**exactly three input variables are 1s. Also draw logic circuit diagram. (Attach Simulated**

**circuit diagram as well).**

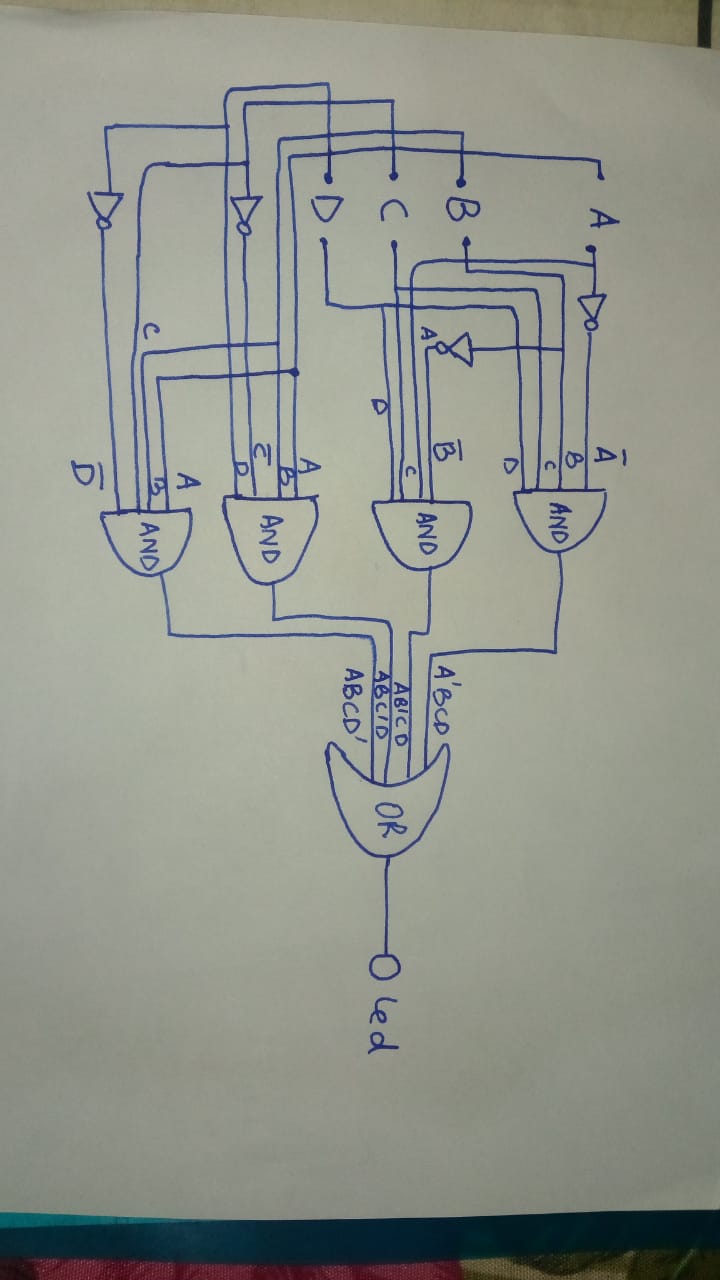
* **TRUTH TABLE :**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **OUTPUT** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **0** |
| **0** | **1** | **0** | **0** | **0** |
| **0** | **1** | **0** | **1** | **0** |
| **0** | **0** | **1** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **1** | **0** | **0** |
| **0** | **1** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** | **0** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **1** | **0** | **0** | **0** |
| **1** | **1** | **0** | **1** | **1** |
| **1** | **0** | **1** | **0** | **0** |
| **1** | **0** | **1** | **1** | **1** |
| **1** | **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** | **0** |

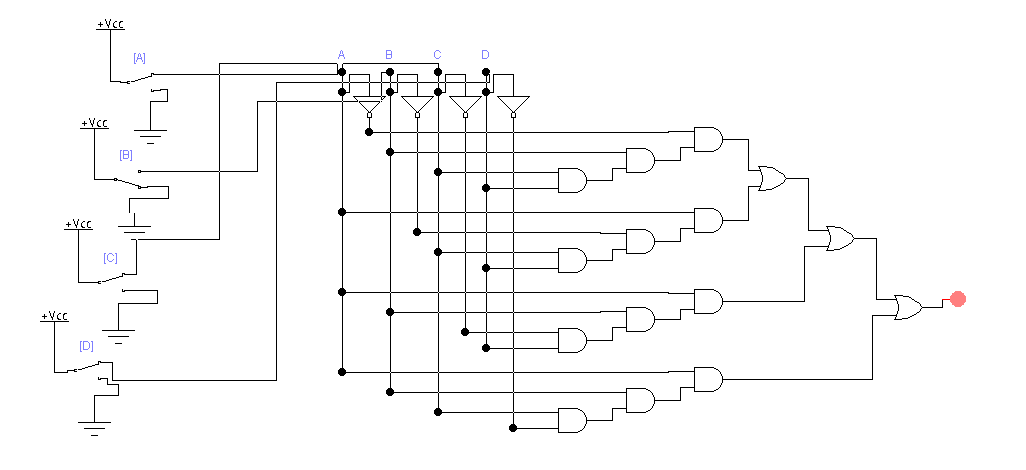
* **BOOLEAN EXPRESSION:**

A’BCD + AB’CD + ABC’D + ABCD’

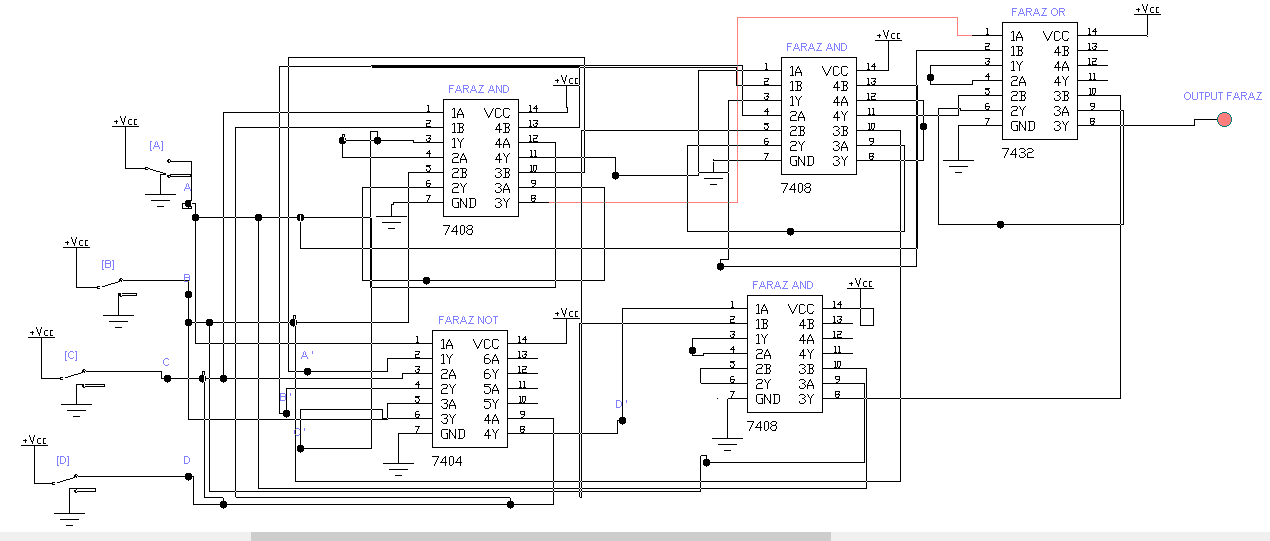
* **CIRCUIT DIAGRAM USING 4-INPUT GATES:**

****

* **GATE-LEVEL SIMULATION CIRCUIT:**



* **IC-LEVEL SIMULATION CIRCUIT:**



* **VERIFICATION OF BOOLEAN EXPRESSION USING LOGIC CONVERTER:**

